MAINBOARD TRACKS CUT LIST - SIDE 1

	CONNECTION BEING CUT			
CUT#	**FROM (OUT) chip/pin (signal, part)**	**TO (IN) chip/pin (signal, part)**	**COMMENT**	**IMPORTANCE**
1 (rev.3)	U87/11 (should be NSO, 7400) pag.51	U86/11 (7407) pag.53	Wrong connection on the original PCB. On the original mainboard PCB, gate U87/13,12,11 was connected between U85/12 and U86/11 as an inverter for signal I between U85 and U86. That was wrong and this cut restores the (correct) original schematics. See also cuts #20 and #24 on side 2.	Critical. Affecting video. Affecting RS232.
2 (rev.3)	U79/10 (SO, 8255) pag.50	R87/1 (SO, RS232 out) pag.51	Wrong connection on the original PCB. SO being fed directly to R87/1. SO was connected directly to R87, instead of being routed through an inverter (gate U87/11,12,13, see pag. 51). This mistake is here corrected by interrupting SO and then reconnecting it with a wire (#18) to U87/12 on side 2 of the mainboard. This cut is equivalent to cut #20 on side 2. One of these 2 cuts would have been enough.	Medium. Affecting RS232.
3,4	VCC	U89/1 (27512) pag.42	Cut made for the purpose of disconnecting pin 1 of U89 (A15) from VCC and use it to select between two sets of 32KB (2 operating systems) stored in EPROM. This was done manually with a switch. Selection between the two different operating systems (16KB) within one set is made from keyboard in the startup configuration.	Optional. For 64KB EPROM.
5 (rev.3)	R107 (JSC) pag.50	J6/10	The original PCB layout had JSC connected to j6/pin10 but the original manual had JSC listed at j6/pin8. I changed the PCB layout to match the original manual. See wiring #1 on mainboard side 1.	Medium. Affecting Joystick.
6	U56/4 (NOES, 7442) pag.41	U70/12 (NOES, 7442) pag.42	Cut made for the purpose of rerouting NOES directly to the single EPROM chip (27512). If a single chip is used for the Basic memory, there is no need for NOES to be multiplexed through U70. In fact, U70 becomes useless altogether.	Optional. Depending on R/O memory configuration.
7	U56/9 (NCS3, 7442) pag.41	R34/R33 (NCAS DRAM bank #3) pag.43	Cut made for disconnecting DRAM bank #3 from old NCS3 signal for the purpose of the “64KB DRAM memory chips modification”.	Optional. For 64KB DRAM memory chips.
8	U55/6 (NCS0, 7400) pag.41	R26/R25 (NCAS DRAM bank #0) pag.43	Cut made for disconnecting DRAM bank #0 from old NCS0 signal for the purpose of the “64KB DRAM memory chips modification”.	Optional. For 64KB DRAM memory chips.
9	U54/11 (7400) pag.41	U55/5 (7400) pag.41	Cut made for the purpose of inserting a manual switch on the R/O signal for the first 16KB memory area. (under BASIC configuration). The switch is used for making the Basic area R/W under NMI Basic before pushing the NMI button because the CPU state is saved in the Basic memory area since the rest of the memory must be saved unchanged to preserve the original contents of the program being “cracked”.	Optional. For NMI Cracking.
10	U36/9 (LO6, 7474) pag.41	U35/9 (7486) pag.41	Cut made for the purpose of disconnecting U35/9 from LO6, for the purpose of the “80KB memory modification”. Under this configuration U35/9 must be connected to PO instead of LO6.	Optional. For 80KB total DRAM memory.
11 (rev.3)	u74/4 (BA7, 7407) pag.40	JEXA/8 pag.38	Wrong connection on the original PCB. BA7 being connected to the floppy interface through JEXA/8. Correctly, BA1 should be connected to JEXA/8. See also wiring #22 on side 2.	Critical. Affecting Floppy Interface.
12	U13/2 (AC5, 74193), pag.45 U14/2 (AC5, 7410) pag.48	U15/2, (7474) pag.45	On the original mainboard side 1, there is a connection from U13/2 to U14/2,9 and further to U15/2. For the purpose of the “80 chars/line modification” the connection must be cut right next to U15/2, preserving the connection between U13/2 and U14/2,9.	Optional. Added for 80 chars per line in CP/M.
13 (rev.3)	GND	R107	Wrong connection on the original PCB. On the original mainboard, R107 is wrongfully connected to GND instead of VCC. This cut separates R107 from GND and then wiring #19 on side 2 restores connection to VCC.	Medium. Affecting Joystick.
14	VCC	U24-31/9	16KB DRAM chips (KP565PY6) have pin 9 N.C.; 64KB DRAM chips (KP565PY5), on the other hand, have pin 9 working as address line A7. On my working mainboard I used 64KB DRAM chips in DRAM bank #0 (right above the video memory, bank #1). The original mainboard had pins 9 of U24-31 (bank #0) connected to VCC and then on the back of the board resistors R10-17 (see pag.40) were connected to VCC on pins 9 of U24-31. Now that I used 64KB DRAM chips for bank #0 (“64KB DRAM chips modification”) R10-17 had to be disconnected from pins 9 of DRAM bank #0 and rewired to VCC somewhere else. See cuts #A0-A6 on side 2 of the mainboard and cut #A7 on side 1. See also wirings #A0-A7 on side 2 of the mainboard.	Optional. For 64KB DRAM memory chips.
A7	U24-31/9 (N.C., 4116)	R17/VCC	SEE COMMENTS ABOVE	Optional. For 64KB DRAM memory chips.

NOTE:

There are 3 possible modifications considered here, all applied to the original schematics (after of course all the critical important changes (bugs shown in color on the last column) have been made so that the design is a working one):

— The “64KB DRAM chips modification”. This consists of all changes required for the computer to use one single DRAM bank of 64KB chips instead of three separate banks (#0, #2, #3) of 16KB chips. Under this configuration the computer does NOT use the whole 80KB total DRAM available, it only uses 48KB of the new 64KB DRAM bank plus the video memory (DRAM bank #1) which is left unchanged. So the total DRAM memory available to the computer is still 64KB. The new 64KB DRAM bank can be installed in any one of the 3 old banks (#0, #2, #3). This is supposed to use single-voltage DRAM chips only (the original 4116 had 3 different voltages!!!). This change is the absolutely necessary first step towards...

— The “80 KB memory modification”. This consists of all changes necessary (applied after the “64KB DRAM chips modification”) for the computer to be able to address and use the whole 80KB total DRAM installed.

— The “80 chars/line modification”. This makes use of the left&right border area in CP/M enlarging the text area available to max. 80 characters per line.

MAINBOARD TRACKS CUT LIST - SIDE 2

	CONNECTION BEING CUT			
CUT#	**FROM (OUT) chip/pin (signal, part)**	**TO (IN) chip/pin (signal, part)**	**COMMENT**	**IMPORTANCE**
1	U55/11 (CS1, 7400) pag.41	U76/13 (old CS1, 8212) pag.47	The original CS1 signal is disconnected from U76/13 for the purpose of making the "80KB DRAM modification" described on page 54 of the original hardware manual.	Optional. For 80KB total DRAM memory.
2	U55/11 (CS1, 7400) pag.41	U55/10 (7400) pag.41	Cut made for the purpose of disconnecting gate U55/10,9,8 from the rest of the mainboard completely. On my working mainboard this gate was left unused.	Optional.
3	U02/9 (NVMA, 7474) pag.44	U55/9 (7400) pag.41	Cut made for the purpose of disconnecting gate U55/10,9,8 from the rest of the mainboard completely. On my working mainboard this gate was left unused.	Optional.
4	u55/8 (old NCS1, 7400) pag.41	u02/1 (7474) pag.44	This gate (U55/10,9,8) used to generate the NCS1 signal (for video memory) under the 64KB memory configuration. Under the "80KB memory configuration" the NCS1 signal is being generated as described on page 54 of the original hardware manual and therefore the output of this gate becomes obsolete. See also cuts #2 and #3 above.	Optional. For 80KB total DRAM memory.
5 (rev.3)	U36/5 (PO, 7474) pag.41	U36/1 (7474) pag.41	Wrong connection on the original PCB. PO being fed to input U36/1.	Critical. Affecting computer startup.
6	U35/9 (input, old LO6, 7474) pag.41	U52/2 (input, old LO6, 7410) pag.41	Cut made for the purpose of disconnecting U35/9 from U52/2. The original schematics had these two inputs connected to signal LO6 from U36/9. See also cut #10 on side 1 which separates U35/9 from U36/9 (LO6). This cut is equivalent to cut #9. One of them would have been enough.	Optional. For 80KB total DRAM memory.
7	U71/12 (BA14, 7407) pag.40	U35/2 (7486) pag.41	Cut made for the purpose of disconnecting U35/2 from signal BA14. U35/2 will be then routed to U36/6 (NPO) so that gate U35/1,2,3 will generate function NLO6 xor NPO for further use in the "80 chars/line modification" for CP/M. See also cuts #8 and #10.	Optional. For 80 chars per line in CP/M.
8	U35/3 (AB14, 7486) pag.41	U56/15 (7442) pag.41	Cut made for the purpose of disconnecting U56/15 from signal AB14 and rerouting U56/15 to BA14 directly. Output U35/3 will then be connected to the rest of the extra circuitry that makes up the "80 chars/line modification" for CP/M. See also cuts #7 and #10.	Optional. For 80 chars per line in CP/M.
9	U35/9 (input, old LO6, 7474) pag.41	U52/2 (input, old LO6, 7410) pag.41	The original schematics show U52 as being a 7410 (3 x 3-input NAND) and gate U52/11,10,9,8 connected as inverter between output U52/12 and input U35/1. In reality, the original mainboard had U52/12 directly connected to U35/1 and U52 was thus supposed to be a 7411 (3 x 2-input AND), not a 7410. This cut is made for the purpose of the "80KB memory modification". According to this modification, BA14 goes directly to U56/15 and therefore gates U52/1,2,13,12 and U52/11,10,9,8 and U35/1,2,3 are not used anymore, so U52/2 is isolated by this cut. This cut is equivalent to cut #6. One of them would have been enough.	Optional. For 80KB total DRAM memory.
10	U52/12 (AB1315, 7410) pag.41	U35/1 (input, 7486) pag.41	The original schematics show U52 as being a 7410 (3 x 3-input NAND) and gate U52/11,10,9,8 connected as inverter between output U52/12 and input U35/1. In reality, the original mainboard had U52/12 directly connected to U35/1 and U52 was thus supposed to be a 7411 (3 x 3-input AND), not a 7410. This connection is cut here (cut #10) and gate U35/1,2,3 is then used to generate function NLO6 xor NPO for further use in the "80 chars/line modification" for CP/M, for that reason U35/1 is rerouted to U36/8 (NLO6). See also cuts #7 and #8.	Optional. For 80 chars per line in CP/M.
11	U56/7 (NCS2, 7442) pag.41	R41/R42 (NCAS DRAM bank #2) pag.43	Cut made for the purpose of disconnecting DRAM bank #2 from old NCS2 signal for the purpose of the "64KB DRAM memory chips modification".	Optional. For 64KB DRAM memory chips.
12,13,14, 15,16,17	U70/1,2,7,13,14,15 pag.42		Cut made for the purpose of isolating U70 from the rest of the circuit. U70 is no longer necessary if not using 2716/2732 EPROMs for the Read-Only memory. My working mainboard had one 27512 EPROM for Basic/OPUS/Devil/NMI Basic.	Optional. Only when using a single EPROM for Basic.
18,19	VCC	U89/26,27,28 pag.42	Cut made for the purpose of separating pins 26, 27 and 28 of U89 from one another, as this place on the mainboard was used for a 27512 EPROM (64KB) which held 4 different operating systems (Basic, Basic w/ NMI, Devil, Opus). Pin 28 stays connected to VCC but 27 (A14) and 26 (A13) will be used for selecting one of the 4 operating systems. See also cuts #3 and #4 on side 1, which separate pin 1 (A15) from VCC.	Optional. Only when using a single EPROM (27512) for Basic.
20 (rev.3)	U79/10 (SO, 8255) pag.50	R87/1 (SO, RS232 out) pag.51	Wrong connection on the original PCB. SO being fed directly to R87/1. SO was connected directly to R87, instead of being routed through an inverter (gate U87/11,12,13, see pag. 51). This mistake is here corrected by interrupting SO and then reconnecting it with a wire to U87/12 on side 2 of the mainboard. This cut is equivalent to cut #2 on side 1. One of these 2 cuts would have been enough.	Medium. Affecting RS232.
21	VBB	DRAM0+2+3/1 (VBB)	VBB should be disconnected from single voltage memory chips, even though for them pin 1 is NC anyway (not used).	Minor. Affecting DRAM.
22	R34 pag.43	R33 pag.43	Cut made in order to isolate R34 and use it as a 33Ω resistor between output U58/4 and the 64K DRAM input A7. Same purpose as cut #26.	Optional. For 64KB DRAM memory chips.
23	R91/1 (TI from U92) pag.51	U79/38 (TI, 8255) pag50	Connection interrupted to allow interconnecting another mainboard's tape output (loading signal from a second computer mainboard instead of external tape)	Minor. Added as extra feature.

24 (rev.3)	U85/12 (I, 74157) pag.49	U87/13+12 (should be RS232 out) pag.51	Wrong connection on the original PCB. I being fed to inputs U87/13+12. This cut disconnects I from U87/13+12 and then wiring #21 on side 2 restores I at U86/11 as per the original schematics.	Critical. Affecting video. Affecting RS232.
25 (rev.3)	U85/13 (input B4 of 74157) pag.49	U80/3, U81/11 pag.49	Wrong connection on the original PCB. Direct connection from U81/11 to U80/3 instead a diode between them.	Medium. Affecting Flash feature.
26	VCC pag.43	R34 pag.43	Cut made in order to isolate R34 and use it as a 33Ω resistor between output U58/4 and the 64K DRAM input A7. Same purpose as cut #22.	Optional For 80KB total DRAM memory.
27	U74/6, R70 (BCLK, 7407) pag.40	J8A+B+C/32	Cut made in order to disconnect pin32 of J8A, J8B, J8C (expansion connector) from BCLK. This signal was then generated separately from an extra 7407 chip that had one of the inputs connected to CLK from the mainboard. The chip was simply mounted on top of U74 on my working mainboard. The purpose was to avoid overloading the BCLK signal from the mainboard with any additional circuitry connected to the expansion connector (i.e. external EPROM programmer).	Optional.
28	U70/8, R53 (BNM1, 7407) pag.40	J8C/26	Same as above for BNM1.	Optional.
29	U71/4, R46 (BNIORQ, 7407) pag.40	J8C/24	Same as above for BNIORQ.	Optional.
30	U56/3 (NOEB, 7442) pag.41	U89/22 (input NOE of 27512) pag.42	On my working mainboard I used the mounting space for U23 to install the BOOT EPROM (2716) and the mounting space for U89 to install the BASIC EPROM (that is, the other way around from the original design). In this configuration U70 (7442, see pag.42) becomes useless since there is one single chip for the BASIC EPROM instead of 8. So this cut disconnects U89/22 (where NOEB used to go) from U56/3. See also wiring #5 on mainboard side 1.	Optional. For BASIC EPROM installed in place of BOOT EPROM.
A0	U24-31/9 (N.C., 4116)	R10/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A1	U24-31/9 (N.C., 4116)	R11/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A2	U24-31/9 (N.C., 4116)	R12/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A3	U24-31/9 (N.C., 4116)	R13/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A4	U24-31/9 (N.C., 4116)	R14/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A5	U24-31/9 (N.C., 4116)	R15/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A6	U24-31/9 (N.C., 4116)	R16/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.

MAINBOARD REWIRINGS LIST - SIDE 1

	CONNECTION BEING MADE			
WIRING#	**FROM (OUT) chip/pin (signal, part)**	**TO (IN) chip/pin (signal, part)**	**COMMENT**	**IMPORTANCE**
1 (rev.3)	R107 (JSC) pag.50	J6/8	Wrong connection on the original PCB. The original PCB layout had JSC connected to j6/pin10 but the original manual had JSC listed at j6/pin8. I changed the PCB layout to match the original manual. See cut #5 on mainboard side 1.	Medium. Affecting Joystick.
2	SB/3 (BA11, U74/12) pag.42	SB/4 (pin 23, U89) pag.42	My working mainboard did not have the switch SB installed, instead I just soldered a jumper across pins 3 and 4 of SB mounting holes to connect address BA11 to the 27512 chip.	Optional. Affecting EPROM.
3	VCC	VCC	Wiring made for the purpose of disconnecting pin 1 of U89 (A15 of 27512 EPROM) from VCC and use it as an address line.	Optional. For 64KB EPROM.
4	VCC	VDD	Wiring made for the purpose of transforming the VDD line going to the DRAM chips into a VCC line, which is further used for wirings A0-A7 on mainboard side 2 (I did not used 3-voltage memory chips that the mainboard was originally designed for).	Optional. For single-voltage DRAM chips.
5	U56/3 (NOEB, 7442) pag.41	U23/20 (2716) pag.42	On my working mainboard I used the mounting space for U23 to install the boot EPROM (2716) and the mounting space for U89 to install the BASIC EPROM (that is, the other way around from the original design). In this configuration U70 (7442, see pag.42) becomes useless since there is one single chip for the BASIC EPROM instead of 8. So this wiring is made for the purpose of routing the NOEB signal to U23/20 instead of U89/22. For the same reason, the cut #30 on mainboard side 2 disconnects U89/22 (where NOEB used to go) from U56/3.	Optional. For BOOT EPROM installed as U23.
6	U56/4 (NOES, 7442) pag.41	U89/22 (27512) pag.42	On my working mainboard I used the mounting space for U23 to install the boot EPROM (2716) and the mounting space for U89 to install the BASIC EPROM (that is, the other way around from the original design). In this configuration U70 (7442, see pag.42) becomes useless since there is one single chip for the BASIC EPROM instead of 8. So this wiring is made for the purpose of routing the NOES signal to U89/22 instead of U70/12 where it used to go (see pag. 42).	Optional. For BASIC EPROM installed as U89

MAINBOARD REWIRINGS LIST - SIDE 2

	CONNECTION BEING MADE			
WIRING#	**FROM (OUT) chip/pin (signal, part)**	**TO (IN) chip/pin (signal, part)**	**COMMENT**	**IMPORTANCE**
1 (rev.3)	U36/9 (LO6, 7474) pag.41	U36/1 (7474) pag.41	Wrong connection on the original PCB. This connection already exists in the original schematics, but the original mainboard has a mistake where U36/1 is connected to U36/5 (PO) instead of U36/9 (LO6). See also cut #5 on mainboard side 2.	Critical. Affecting computer startup.
2	U36/9 (LO6, 7474) pag.41	U52/2 (input, old LO6, 7410) pag.41	Because of cut #10 on side 1 and cut #6 on side 2, U52/2 is disconnected from signal LO6. This wiring restores LO6 to U52/2 which is required only for a 64KB total DRAM memory configuration. But since cut #10 on side 1 and cut #6 on side 2 are only required for 80KB total DRAM memory configuration, it looks like this wiring is useless anyway. Its only use was that on my working mainboard it gave a new soldering point for signal LO6 to be further connected by other wires to the extra circuit boards I had added.	None. Useless.
3	U36/8 (NLO6, 7474) pag.41	U35/1 (7486)	Wiring made for the purpose of generating the signal NLO6 xor NPO which is further used in the "80 chars/line modification" circuit. Gate U35/1,2,3 is completely separated from the original schematic and reused to generate this function.	Optional. Added for 80 chars per line in CP/M.
4	U36/6 (NPO, 7474) pag.41	U35/2 (7486)	SAME AS ABOVE	Optional. Added for 80 chars per line in CP/M.
5	U36/5 (PO, 7474) pag.41	U35/9 (7486)	Required for the "80KB memory modification".	Optional. For 80KB total DRAM memory.
6	U36/12 (O6 from U79, 7474) pag.41	U52/4 (7411)	Required for the "80KB memory modification". U52/3,4,5,6 is used to generate an AND function with O6, LO6 and CS1, the result of which is applied to U76/13 (8212) instead of CS1.	Optional. For 80KB total DRAM memory.
7	U36/1 (LO6, 7474) pag.41	U52/3 (7411)	SAME AS ABOVE	Optional. For 80KB total DRAM memory.
8	U55/11 (CS1, 7400) pag.41	U52/5 (7411)	SAME AS ABOVE	Optional. For 80KB total DRAM memory.
9	U52/6 (7411)	U76/13 (8212)	SAME AS ABOVE	Optional. Added for 80KB mem.
10	U71/12 (BA14, 7407) pag.40	U56/15 (7442) pag.41	After cut #8 on mainboard side #2, U56/15 is disconnected from U35/3 and then connected to BA14. Required for the "80KB memory modification".	Optional. For 80KB total DRAM memory.
11	U71/12 (BA14, 7407) pag.40 ---------- OR(!!!) ---------- U56/15 (7442) pag.41	U58/3 (74157) pag.43 ---------- OR(!!!) ---------- U58/3 (74157) pag.43	Required for the "80KB memory modification". (THIS INCLUDES THE ALTERNATIVE BELOW) ---------- OR(!!!) ---------- Required for the "64KB DRAM memory chips modification".	Optional. For 80KB total DRAM ----- OR(!!!) ----- For 64KB DRAM memory chips.

12	U17/12 (VLD from U37/6, 7400) pag.41	U79/25 (input PB7, 8255) pag.50	UNEXPLAINED Maybe some CP/M routines read the Joystick port to detect the “1” level of VLD for some interrupts?? Line PB7 of the Joystick port is not used by the Joystick.	Most likely useless
13	U35/8 (7486) pag.41	U58/2 (74157) pag.43	Required for the “64KB DRAM memory chips modification”.	Optional. For 64KB DRAM memory chips.
14	U58/4 (A7 for DRAM 64K, 74157) pag.43	R34 pag.43	R34 is used as a 33Ω resistor in series with the new address line A7 for DRAM, under the 80KB memory configuration. In this case (my working mainboard) I used DRAM bank #0 for the 64KB DRAM chips and I changed R34 to 33Ω instead of 1KΩ, rewiring it to the new address line A7 for DRAM and to U58/4. Other unused resistor mounting holes could have been used too, R34 is not the only option.	Optional. For 64KB DRAM memory chips.
15	R34 (A7 for DRAM 64K) pag.43	U31/9 (A7, 4164 DRAM chip)	SAME AS ABOVE	Optional For 64KB DRAM memory chips.
16	D16/1 (BA13 from U72/12) pag.40	U89/26 (A13, 27512 EPROM) pag.42	Required for the 64KB BASIC EPROM.	Optional For 64KB EPROM.
17	U79/10 (SO, 8255) pag.50	U89/27 (A14, 27512 EPROM) pag.42	Required for a >=32KB BASIC EPROM. For 32KB EPROM, selection between the two 16KB operating systems is made by the software in the BOOT EPROM via user choice from keyboard. For 64KB EPROM, the selection between two sets of 2 operating systems is made manually with a switch.	Optional For >=32KB EPROM.
18 (rev.3)	U79/10 (SO, 8255) pag.50	U87/12 (7400) pag.51	Wrong connection on the original PCB. SO being fed directly to R87. SO was connected directly to R87, instead of being routed through an inverter (gate U87/11,12,13, see pag. 51). This mistake is corrected by interrupting SO (see cuts #2 on side 1 and #20 on side 2) and then reconnecting it here with a wire to U87/12 on side 2 of the mainboard. See also #20 below.	Medium. Affecting RS232.
19 (rev.3)	VCC	R107	Wrong connection on the original PCB. On the original mainboard, R107 is wrongfully connected to GND instead of VCC. This wiring restores connection to VCC. See also cut #13 on side 1.	Medium. Affecting Joystick.
20 (rev.3)	U87/11	R87	Wrong connection on the original PCB. SO being fed directly to R87/1. SO was connected directly to R87, instead of being routed through an inverter (gate U87/11,12,13, see pag. 51). This wiring restores connection between U87/11 and R87 as per the original schematics. See also wiring #18 above.	Medium. Affecting RS232.
21 (rev.3)	U85/12 (I, 74157) pag.49	U86/11 (7407) pag.53	Wrong connection on the original PCB. I being fed to inputs U87/13+12. This wiring restores I at U86/11 as per the original schematics. See also cut #24 on mainboard side 2.	Critical. Affecting video.
22 (rev.3)	U73/4 (BA1, 7407) pag.40	JEXA/8 pag.38	Wrong connection on the original PCB. BA7 being connected to the floppy interface through JEXA/8. Correctly, BA1 should be connected to JEXA/8. See also cut #11 on side 1.	Critical. Affecting Floppy Interface.
23	VCC	U23/21 (VPP/A11, 2716) pag.42	During nomal use, VPP should be connected to VCC.	Minor. Affecting BOOT EPROM
24 (rev.3)	U34/8 (NVS, 7420) pag.48	JEXA/9 pag.38	Missing connection on the original PCB. The original hardware manual has JEXA/9 listed as connected to a signal “SI/TRG3” which is supposed to come from the mainboard somewhere. But the signal does not exist anywhere in the original schematics. My working mainboard has this wiring on side 2 going from U34/8 to a via that seems connected to an “attempt” of a track. The via is further connected on side 1 eventually reaching JEXA/9. I would conclude there is actually a missing track on the original mainboard layout that is being restored by this wiring and that JEXA/9 should be listed as connected to NVS.	Critical. Affecting Floppy Interface.
25 (rev.3)	GND	U83/6,7 pag.49	Missing connection on the original PCB. The original schematics show U83/6,7,8 connected together, but the original mainboard layout only has U83/6,8 connected together without them being further connected to pin 7 (GND).	Critical. Affecting video.
A0	VCC	R10/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A1	VCC	R11/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A2	VCC	R12/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A3	VCC	R13/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A4	VCC	R14/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A5	VCC	R15/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A6	VCC	R16/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.
A7	VCC	R17/VCC	SEE COMMENTS FOR CUT #14 ON SIDE 1	Optional. For 64KB DRAM memory chips.